REMARKS/ARGUMENTS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-15 are pending in the application, with Claims 1, 5, 9 and 13 amended by the present amendment.

In the outstanding Office Action, Claims 1-3 were rejected under 35 U.S.C. §103(a) as being unpatentable over Butta' et al (U.S. Patent No. 6,633,939; hereinafter Butta') in view of Watts (U.S. Patent No. 6,647,449; hereinafter Watts); Claims 5-8 and 13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Butta' in view of Kurth (U.S. Patent No. 6,880,028; hereinafter Kurth); Claims 9 and 11-12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Butta' in view of Kenny (U.S. Patent No. 6,393,506; hereinafter Kenny); and Claims 4, 10 and 14-15 were indicated as containing allowable subject matter.

Applicants acknowledge with appreciation the indication of allowable subject matter.

Applicants acknowledge with appreciation the personal interview between the Examiner, the Examiner's supervisor and Applicants' representative on May 24, 2005. During the interview, the Examiners indicated that amending Claim 1 to recite that the masked check result and the check result are consecutive data would overcome the art of record. The Examiners also indicated that amending Claim 5 to recite upping a level of priority information during a round of arbitration would overcome the outstanding rejection. The Examiners further recommended that Claim 5 be amended to depend from amended Claim 1. The Examiners further indicated that amended Claims 9 and 13 distinguished over the art of record.

Claim 1 is amended cosmetically to recite that the masked check result and the check result are consecutive data would overcome the art of record. Support for this amendment is

found in Applicants' originally filed specification.[1] Claim 5 is amended to more clearly describe and distinctly claim Applicants' invention. Support for this amendment is found in Applicants' originally filed specification.[2] Claim 5 is further amended to depend from Claim 1. Claim 9 is amended to clarify that the claimed operating frequencies are processor operating frequencies. Support for this amendment is found in Applicants' originally filed specification.[3] Claim 13 is amended to recite that the priority generating circuit comprises a plurality of priority information set in advance corresponding to each of a plurality of conditions of a corresponding bus master, and outputs an element of said plurality of priority information when a condition of said corresponding bus master changes. Support for this amendment is found in Applicants' originally filed specification.[4] No new matter is added.

Briefly recapitulating, Claim 1 is directed to an arbitration circuit including, inter alia, a round robin block. The round robin block includes a) a round robin control unit for determining, through round robin control, a priority order of the bus access requests from the plurality of bus masters, and b) a round robin masking unit for masking data of the check result with mask data to output a masked check result. The mask data is generated on the basis of the priority order. The masked check result and the check result are consecutive data. Applicants claimed circuit allows for fair bus access by ensuring low priorities are not left without ever being awarded any opportunity for bus access.[5]

As acknowledged in the Official Action, Butta' fails to disclose Applicants' claimed round robin block. The Official Action cites Watts for a disclosure of a circuit for performing round robin arbitration.[6] However, as noted in the interview, Watts does not

[1] Specification, Claim 4.
[2] Specification, page 21, line 9 – page 25, line 20.
[3] Specification, page 25, line 21 – page 29, line 17.
[4] Specification, page 26, lines 5-22.
[5] Specification, page 2, lines 5-11; page 14, line 9-11; page 14, line 19 – page 15, line 1.
[6] Watts, column 3, line 4 – column 4, line 54.

disclose or suggest a masked check result and a check result that are arranged consecutively. In Watts, priority data and mask data is OR'ed in reduction OR device 50.

Claim 5, now dependent on Claim 1, further recites that the plurality of bus masters each comprise a priority generating circuit for generating the priority information, and the plurality of priority generating circuits are each configured to up a level of priority information during a round of arbitration when a bus access request from the corresponding bus master is unaccepted during a previous round of arbitration.

As acknowledged in the Official Action, Butta' fails to disclose Applicants' claimed up the level of the priority information when a bus access request from the corresponding bus master is unaccepted. Kurth describes a method and system for dynamically changing the priority of requests over time.[7] However, as acknowledged during the interview, Kurth ups requests based on a timer and does not up a request based upon a decision in a previous round of arbitration as recited in Applicants' amended Claim 5.

Claim 9 recites, inter alia, when a processor operating frequency of a corresponding bus master is changed, the priority generating circuit outputs one of pieces of priority information that correspond respectively to a plurality of processor operating frequencies. As acknowledged in the Official Action, Butta' fails to disclose Applicants' claimed priority generating circuit outputs one of pieces of priority information that correspond respectively to a plurality of operating frequencies. Kenny describes "In a fixed priority scheme which may be used in combination with either the preemptive or conditional priority types, each I/O module is assigned a fixed priority. By comparison, a dynamic allocation priority scheme shifts priorities among the various I/O modules according to a predetermined or pre-defined protocol. For example, a statistical weighting priority scheme may assign a higher priority to those I/O modules consistently requesting the largest amount of data or requesting data more

[7] Kurth, column 5, lines 17-27.

frequently. Priority is dynamically allocated to those modules as these weightings change over time."[8] However, as acknowledged during the interview, Kenny fails to disclose or suggest outputting priority information that corresponds respectively to a plurality of processor operating frequencies.

As noted previously, Claim 13 is amended to recite that the priority generating circuit that comprises a plurality of priority information set in advance corresponding to each of a plurality of conditions of a corresponding bus master, and outputs an element of said plurality of priority information when a condition of said corresponding bus master changes. Butta' describes a bus access arbitration access scheme.[9] However, as suggested by the Official Action, Butta' fails to disclose or suggest Applicants' claimed priority generating circuit which outputs one of pieces of priority information that correspond respectively to a plurality of conditions when a condition of a corresponding bus master is changed. Kurth describes a system and method for dynamically determining/varying the priority of requests.[10] However, Kurth fails to disclose or suggest a priority generating circuit that comprises a plurality of priority information set in advance corresponding to each of a plurality of conditions of a corresponding bus master, and outputs an element of said plurality of priority information when a condition of said corresponding bus master changes.

MPEP §706.02(j) notes that to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Also, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found

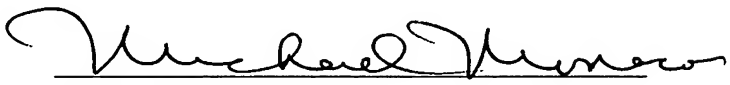
[8] Kenny, column 3, lines 54-65.
[9] Butta, column 3, line 33 – column 4, line 56.
[10] Kurth, abstract.

in the prior art and not based on applicant's disclosure. *In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Without addressing the first two prongs of the test of obviousness, Applicants submit that the Official Action does not present a *prima facie* case of obviousness because both each of the cited references fail to disclose all the features of Applicants' claimed invention.

Accordingly, in view of the present amendment and in light of the previous discussion, Applicants respectfully submit that the present application is in condition for allowance and respectfully requests an early and favorable action to that effect.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Michael E. Monaco
Registration No. 52,041

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)
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